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Heterogeneous Avionics Network Performance Evaluation

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***Abstract*— New aircraft generation uses heterogeneous embedded architecture based on a backbone network AFDX (Avionics Full Duplex Switched) providing communications between critical avionics systems and peripheral networks for data acquisition. In this study, we investigate the real time performance evaluation of such heterogeneous network. The goal of this paper is to carry out a case study based on a local bus ARINC 825 (CAN BUS) interconnected to an AFDX network via specific Gateway Modules. We make an analysis of the processing and transmission delays per device. We study the use of gateway nodes, their functionality and their processing delay. Data exchanged experience a variant delay in their passage through these intermediaries, which influences the global latency. Approaches that have already been conducted for a homogeneous AFDX network to evaluate communication latencies must be generalized in the context of a global heterogeneous network.**

***Keywords*— heterogeneous embedded networks, AFDX, ARINC 825, CAN, gateway, performance analysis**

I. INTRODUCTION

Avionic embedded network architectures are currently experiencing major changes. Aircraft tend to be more electronic with the larger use of on-board microprocessors. Data flow between systems and the number of connections between functions will, therefore, be increased.

Thus, new requirements in embedded networks have emerged (centralization, determinism, higher rate, etc.). Several solutions have been proposed to answer these requirements. Among these solutions, is the Avionics Full DupleX switched ethernet (AFDX) [1] which represents a redundant and reliable ethernet network [2], [3] developed and standardized by the European industrial avionics and in particular by Airbus.

In fact, nowadays aircraft have a completely new architecture that integrates different fields, applications, and heterogeneous network. The last consists of different sub-heterogeneous networks (field busses, traditional avionics protocol such as ARINC 429 [4], sensor networks, open world network, Controller Area Network CAN [5] etc.), interconnected to the federator avionic technology AFDX .

Real-time performance evaluation methods are made for homogeneous avionics networks in several researches [6]-[11], especially for AFDX network.

Furthermore, currently networks are complex heterogeneous systems. This heterogeneity requires even more a real assessment of the Quality of Service (QoS) metrics in terms of delay, jitter, bandwidth, message loss, integrity, etc. It includes the performance analysis of the bridging strategy between the different technologies. Therefore, design certification and network performance analysis require new study techniques.

In this purpose, this study focuses on the area of real-time performance evaluation of heterogeneous avionics networks. We consider a heterogeneous network architecture that is already integrated into the aircraft AFDX- ARINC 825 [12]. Flows are transmitted by more than one technology. Thus, we analyze, in this paper, the end-to-end delays over such a heterogeneous path.

The manuscript is composed as follows. The next section details the AFDX network system characteristics. The third section presents timing verification approaches for homogeneous avionics network. Then, in the fourth section, the heterogeneous avionics network is described. The avionics case study is presented and the end-to-end delay is analysed. Finally, we conclude the work in section five.

II. OVERVIEW OF AN AFDX HOMOGENEOUS NETWORK

AFDX technology [1]-[3] brings a number of improvements such as higher data speed transfer and much less wiring, thus improve determinism and guarantee bandwidth.

AFDX is a standard that defines the electrical and protocol specifications (IEEE 802.3 and ARINC 664, Part 7) for exchanging data between avionics subsystems. It is used as the main avionics data bus network. Based on commercial 100 Mbit/s switched Ethernet, AFDX uses a special protocol for deterministic timing and redundancy management to provide secure and reliable communications of critical and non-critical data.

when an application sends a message from the source sub-system to the destination application, the source end system, AFDX switch and end system destination are configured to deliver the message to the appropriate ports.

The inputs and outputs of the networks are called End Systems (ES) which are interconnected by switches. Each end system is connected to exactly one port of an AFDX switch and each port of an AFDX switch can be connected at most to one end system. All the end systems and switches support First-In-First-Out (FIFO) queuing. All the links in the network are full-duplex.

A. *Virtual Link*

Virtual Links (VL) [1], [2] standardized by ARINC-664 are the central feature of an AFDX network. A VL is a virtual logic connection with a unicast source and multicast destination.

For the purpose of determinism, virtual links specify a static path for each data flow. Data is transmitted according a Virtual Link Identifier VLID.

A VL is characterized by two parameters to describe the performance:

- Bandwidth Allocation Gap (BAG): is the primary bandwidth control mechanism. The minimum time interval between consecutive frames of the corresponding VL (fig 3), is a power of 2 value in the rank [1,128],
- Minimum and Maximum Frame Length (Smin and Smax): the Ethernet frame length adopted by AFDX is between 64Kb to 1518Kb.

B. *Sub-Virtual Links*

A virtual link can be composed of a number of Sub-Virtual Links Each Sub-VL [1], [2] has:

- a dedicated FIFO queue,
- a round robin algorithm working over IP fragmented packets.

C. *AFDX End System*

The end system ES is the AFDX element which provides an "interface" between the subsystems and avionics AFDX interconnection (fig 1).

An ES receive messages in it communication ports from avionics devices, encapsulating them within UDP, IP, and Ethernet headers and placing them on their adequate Virtual Link queue.

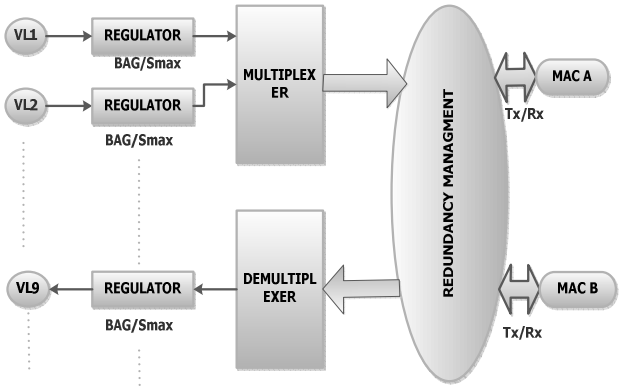

Fig 1: End system model

D. *AFDX Switch*

The switch is the most important equipment in AFDX network defined by the standard 802.1D [13]. Each switch has to filter, police, and mainly forward the arriving packets their destination addresses throw its appropriate ports as shown in Fig 2. The switch examines a forwarding table to determine the corresponding Tx port for every Rx packet according to the correspondent VLID.

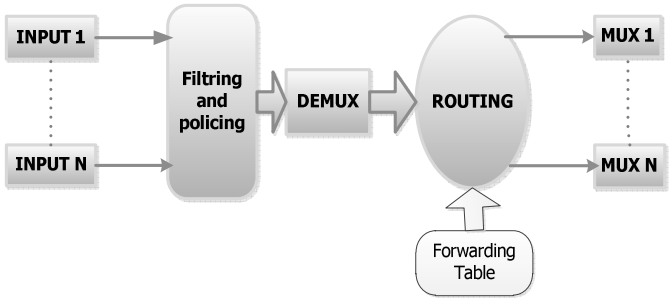

Fig 2: AFDX Switch model

E. *Frame Format*

The AFDX frame format is described in Table 1. The destination and source addresses contain the MAC addresses for the ES. The MAC destination address carries the VLID in the last 16 bits. IP address information is contained in the IP Structure block. The UDP structure identifies the appropriate application port. The AFDX payload ranges from 17 to 1471 bytes.

TABLE I: Frame format

7 bytes	1 byte	6 bytes	6 bytes	2 bytes	20 bytes	8 bytes	17 to 1471 bytes	1 byte	4 bytes	12 bytes
Preamble	Start Frame Delimiter	Destination Address	Source Address	Type IPv4	IP Structure	UDP Structure	AFDX Payload	Seq Number	Frame Check Seq	Interframe Gap

F. *Maximum Jitter*

The jitter is defined as the difference between the beginning of the BAG and the first bit of the frame being sent (fig 3).

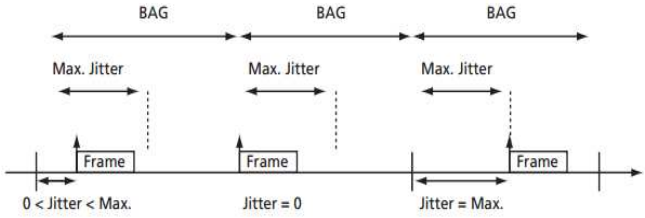

Fig 3: BAG and Jitter

To guarantee determinism, the maximum allowed jitter on each VL at the output of the end system should respect the two following formulas:

$$Max.Jitter \le 40\mu s + \frac{\sum_{i \in \{set of VLS\}} \left(20bytes + L_{MAX}\right) \times 8}{N_{BW}}$$

$$MAX.Jitter \le 500\mu s$$

Where:

- N_{BW} is the speed of the Ethernet link in bits/s
- 40 µs is the typical minimum fixed technological jitter
- 500 µs is the total jitter that is allowed to exceed

III. TIMING VERIFICATION APPROACHES FOR HOMOGENEOUS AVIONICS NETWORK

Since the seminal work of Erlang, Many methods network for performance measurement have emerged to design, guarantee the quality of service and evaluate time performance for a given network.

These methods are classified into two main groups: methods based on simulations and others called analytical.

A. Simulation Method

The simulation [6], [14]-[16] allows approximation of the real network behavior. This approach needs a realistic model based on queuing theory. It allows calculating end-to-end delay on all possible scenarios for a given flow.

The guided simulation approach seeks to assess the pessimism bounds computed using network calculus, in determining a distribution of end-to-end delay. The combinatorial parameters of a network are too large to run all scenarios in a reasonable time. For a given VL, the approach provides a ranking of the other VL according to their degrees of interaction with one being analysed. Then, it consists on scenarios simulation involving VL that has a significant influence on it.

This approach allows taking into account configurations of industrial network size. However, for simulation, we must gain sufficient confidence in the sense that all the scenarios retained after the method application are representative and provide a valid distribution delays throughout.

Several discrete events network simulators were used in the literature for simulation of a homogeneous AFDX network (eg. NS2, NS3, Opnet, QNAP2) [6], [14]- [16].

B. Analytical Method

Analytical methods are based on mathematical models to extract performance criteria. Among these methods, there are deterministic and probabilistic techniques. The first techniques compute conservative bounds for parameters they evaluate; while the second techniques provide all possible parameters values matching probabilities of achieving them.

1) Mathematical Bounds

Two methods are used for the deterministic bounds computing: the network calculus [7], [17], [18] and the trajectories method [8], [19].

Both are based on assumptions on the VLs network inputs:

- There is no assumption on the frame scheduling at the end system level. All VLs are asynchronous,
- the worst case is considered; for each VL, one frame with maximum length S_{max}; is transmitted at each BAG.

This approach is a pessimistic analysis, since it is based on pessimistic assumptions. Indeed, all these methodologies have complementary probabilistic extensions [9]: a probabilistic upper bound has been calculated for the crossing time. These extensions are based on the same assumptions used on the network calculus and the trajectories methods. Thus, they don't solve the problem of pessimism results.

2) Checking Model

This approach is theoretically the only ones that can lead to delays suffered by all the VL frames and their distribution. In particular, the bounds are calculated using the exact model checking and especially its variant delay has been considered for the verification of distributed embedded systems properties. Model checking is an analytical approach that allows determining the exact worst case end-to-end delay and corresponding scenario. This formal method based on automata, explores all possible states of the system. Communication resources are modelled as queuing systems with deterministic memory size bounded using timed automata [10].

3) Stochastic Approach

This approach [11] allows the distribution of end-to-end delay for a given path of a VL. It has been studied for flows to a single switch, and then generalized to the case of a stream to multiple switches. In fact, this method has been validated for both switches and should be generalized to any number of switches.

The resulting distribution is pessimistic compared with the network behavior calculated by the model checking and estimated by a simulation approach. But, it is much less pessimistic than the upper bound obtained by the deterministic network calculus approach.

Its results are interesting and it is complementary to the simulation method.

Also, this approach has been extended to be used for heterogeneous flows (audio, video, etc.) with a static property.

IV. HETEROGENEOUS AVIONICS NETWORK

A. Overview

The evolution of the avionics embedded systems and the amplification of the integrated functions number in the current aircraft imply a huge increase in the exchanged data quantity and thus in the number of connections between functions.

All these innovations involve a significant increase in the complexity of electronic controls, and in the number of actuators and sensors. Therefore, the volume of digital data exchanged between avionic systems is growing and becoming harder to handle.

To control this complexity, new avionics architectures, called Integrated Modular Avionics (IMA), as described in the ARINC 653 standard, have been designed to improve the efficiency in the whole avionic system.

In fact, nowadays aircraft have a completely new architecture that integrates different fields, applications, and heterogeneous networks. The last consists of different sub-heterogeneous networks (field busses, traditional avionics protocol such as ARINC 429 [4], sensor networks, open world network, etc.), in addition to the federator avionic technology AFDX.

The heterogeneity of such interconnection system involves different needs in terms of delay, jitter, bandwidth, message loss, integrity and QoS. Therefore, it requires gateways to solve the problem of different avionics busses dissimilarity.

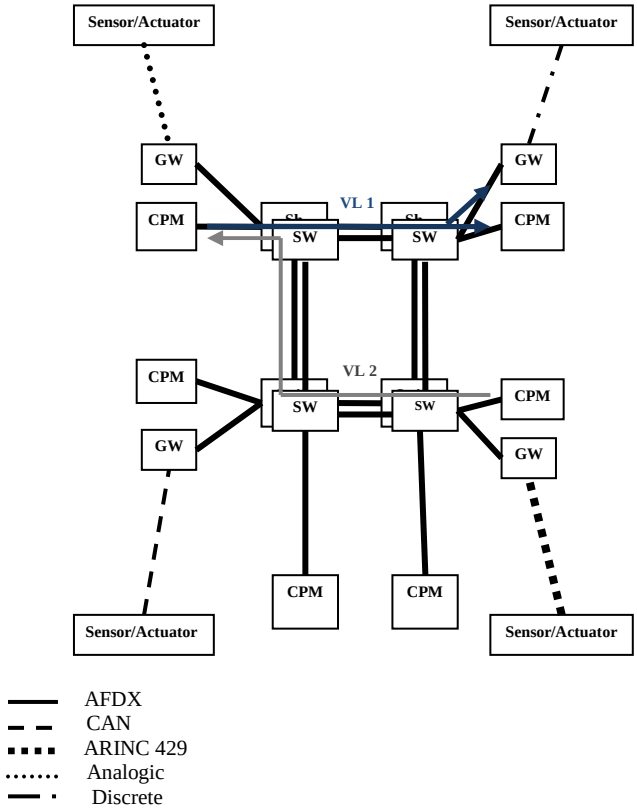

Fig 4: Composition of an Avionics system

Fig 4 shows a model of an ADCN network. An IMA system is composed by:

- Shared computing resources : modules in charge of the execution of applications (Core Processing Modules (CPM), Line Replaceable Units (LRU)),
- Multiplexed avionics communications network, depending on the technology used by different manufacturers, diffusion bus (ARINC 629 or MIL-STD 1553B), or deterministic switched ethernet connected by AFDX SWitches (SW),
- Elements located outside the IMA connected to the avionic word by field busses (analogical, discrete, ARINC 429, CAN),
- Gateways (GW) modules (i.e. Input/Output Modules (IOM) or Common Remote Data Concentrator (CRDC)) for messages transmission between the AFDX basic network and the peripheral communication busses.

B. Case Study: AFDX-ARINC 825(CAN Bus)

This case study is illustrated by Fig 5 that represents a heterogeneous avionic network consisting of the following sub-systems:

- AFDX network: AFDX ES interconnected by AFDX SW
- GW that allows the communication between the avionics world and the peripheral network (sensor network, open world, etc.)
- CAN busses: CAN [5], [20] is used for data acquisition from sensors or for data transmission to the actuators

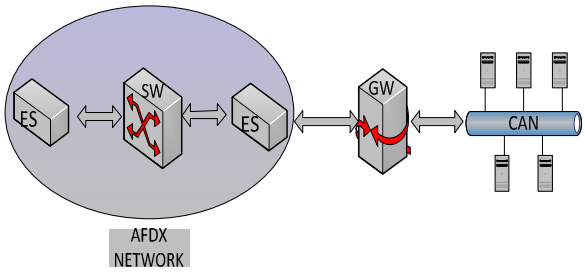

Fig 5: Heterogeneous AFDX- CAN

We have chosen this case study due to the following advantages:

AFDX and ARINC 825 [12], [21], [22] are among the most promising technologies available for the aerospace industry to solve the previous mentioned problems. Indeed, they provide large bandwidth and a network structure that allows wiring reduction while guaranteeing high reliability.

Current air-transport aircraft system architectures have incorporated CAN as an auxiliary sub-system to the AFDX network. Actually, CAN increasingly found its way into aerospace applications thanks to its low cost and efficient networking capability for LRUs that may share data across a common media. Moreover, CAN physical layer protocol specification provide error recovery and protection mechanisms making it attractive to aviation applications.

Nowadays, general aviation system architectures employ CAN as one of the major avionics networks. It is used to link sensors, actuators and other types of avionics devices that typically require low medium data transmission volumes during operation.

1) CAN Characteristics

CAN has to fulfil all requirements of a critical network flight safety to be adapted to the airborne environment.

At the airplane level, there is a need to standardize aspects of the protocol at the system level to ensure interoperability across system and network domains.

These needs were met first by the CAN aerospace standard, which was established in 1998 and is widely used within the general aviation world.

Arising from significant problems trying to integrate systems based on differing CAN application layers; Airbus and Boeing teamed up and initiated the CAN Technical Working Group of the Airlines Electronic Engineering Committee to define the Arinc 825 standard which was published in November 2007. Both leading air framers identified CAN as an important baseline network for their future air planes. The target of Arinc 825 is to ensure interoperability and to simplify

interoperation of CAN sub-systems with other airborne networks.

2) Gateway node

GW is defined as the bridges between two protocols and modules that are connected to the network. These gateway nodes have a generic structure to support different protocols and also several types of sensors and actuators.

The avionic gateways are distributed in the plane (side wings in the cockpit...,) close to sensors and effectors in order to reduce the overall weight of wiring.

These nodes are used to convert the no-AFDX parameters in AFDX parameters and vice versa. The GW is the access point to the ADCN network for other technologies (CAN, A429, and Analogical/Discrete network).

As these networks have different rate characteristics, maximum packet size (MTU), packet priorities, addressing schemes etc, the gateway nodes are designed for heterogeneous embedded protocols which will allow these networks to communicate with each other with the help of different translation functions.

The GW has principally to perform protocol conversion which includes extracting the payloads of the incoming messages and then adding the correct protocol headers before sending them to their destination network.

C. Case Study Performance Evaluation

When communication across gateway nodes takes place in a heterogeneous embedded networks system, the investigation of the end-to-end delay from start to end becomes necessary to guarantee performance.

Thus, the approaches described on section III, which have already been made to the homogeneous network AFDX for the communication latencies analysis, should be extended and generalized to a global heterogeneous network.

The study of a communication medium determinism, in particular temporal determinism, requires the end-to-end latency evaluation: the delay between the message input in the communication stack of the transmitter module (Network 1) and the outlet in the communication stack of the receiver module (Network 2). The determination of an upper bound of the end-to-end latency is a major constraint in the certification process.

If it appears that the estimation of end-to-end latency through IMA must be comprehensive, this assessment, however, faces problems of complexity induced precisely by global character.

So, the study of such an heterogeneous network and the analysis of the gateways characteristics and their impact on the performance of end-to-end delay becomes a major challenge in the design process of heterogeneous embedded systems. However, the few studies focusing on avionics heterogeneous networks have ignored the impact of gateways on the system performance [23]-[25]. Therefore, we have chosen to focus on the study of heterogeneous network, taking into account the impact of the interconnection equipments on end-to-end time system performance.

1) Gateway impact on the end- to-end delay

A gateway approach for achieving semantic interoperability becomes complex and may require long processing times. These delays are equal to the payload extraction and mapping latency.

The gateway mapping strategy according to their functions affects the duration of the message latency at the gateway. So, this duration cannot be considered constant, and the determination of such a delay is necessary for the end to end delay evaluation of a global system.

Gateway uses the most common queuing algorithm FIFO. The latency on the gateway may be defined as:

$$D_{GW} = D_{Rx} + D_{O.GW} + D_{Tx}$$

Where:

- D_{Rx} is the delay that an incoming message has to wait until the message is served from the input buffer
- $D_{O.GW}$ is the gateway operating time
- D_{Tx} is the delay until an outgoing message on the output buffer can be sends in the destination domain

2) AFDX end to end delay analysis

Fig 6 illustrates an AFDX configuration.

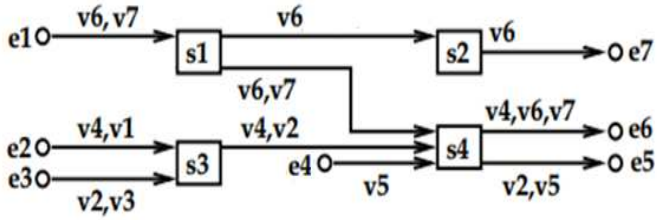

Fig 6: An illustrative AFDX configuration

The AFDX end-to-end delay may be determinated as following:

$$D_{AFDX} = D_{ES} + \left(nb_l \times D_l\right) + \left(nb_{SW} \times t_{SW}\right) + \sum_{SW \in \{setofswitches\}} D_{SW}$$

Where:

- D_{ES} is the delay in the source end system output buffer, nb_l is number of links on a VL path
- D_l is the transmission delay over a link
- nb_{SW} is number of switch on a VL path
- t_{SW} is the delay in a switch from an input port to an output port is considered as a constant = 16µs
- D_{SW} is the delay in SW output port buffer

3) Global end-to- end delay definition

Indeed, the end-to-end delay (D_{eed}) becomes:

$$D_{eed} = D_{AFDX} + D_{GW} + D_{ARINC825}$$

Where:

- D_{AFDX} is the end to end delay for a given AFDX message crossing the AFDX network, which may be calculated using timing performance approaches described in section III

- D_{GW} is the duration a frame might be delayed in the gateway
- $D_{ARINC\ 825}$ is the propagation time across the ARINC 825 bus for a given message to be received by the gateway from a sensor or to be transmitted from the gateway to an actuator

V. CONCLUSIONS

In this paper, we analyse the heterogeneous avionics networks in order to define, as realistic as possible, a real-time performance evaluation. Therefore, the end-to-end delay must take into account the impact of the interconnection equipments.

To evaluate the global network (AFDX-Gateway-ARINC825), we propose to opt for the simulation approach. This constitutes the objective of our running work.

Moreover, the optimization of an avionic gateway can be considered to improve the avionic network real-time performance.

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